Taiwo Raphael Alabi, Ph.D

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Educational/Professional Summary

- Ph.D Materials Science and Engineering- Polymer and Fiber Engineering- Georgia Institute of Tech.
- Process Technical Development Engineer – Senior Integration Engineer on Memory Technologies (3D-NAND)—Modeling, Simulation and Electrical Layout/Design for predictive Electrical Yield/EM and Rel. Fails @probe.
- Process Technical Development Engineer – Back-End Integration Engineer for the embedded Dynamic Random Access Memory (e-DRAM) Technology node.
- Process Technical Development Engineer – SOC Back-End Integration Engineer for the IOT Technology node.
- Process Technical Development Engineer – Far Back-End Integration Engineer- Packaging & Die-Prep for the IOT Technology.
- Process Technical Development Engineer – Yield Analysis for the e-DRAM technology node
- Ph.D Thesis - Design of Photo-modifiable Material Systems for Mask-less Patterning of Functional Ceramic and Metallic Materials at Multiple Length Scales

Objective

Obtain a Technical Consultancy Position utilizing 3.5 years of industrial experience in the areas of SOC Micro-processor fabrication on 14nm/22nm technology nodes with a wealth of expertise in R&D and debugging issues on Cu dual/single damascene processes, packaging and die-prep for current and future SOC and stand-alone processors and memory devices/architectures. Programming and big-data analytics expertise through JMP, JSL scripting, Visual-Basic scripting and Python programming.

Education and Certification

- Ph.D Materials Science and Engineering- Polymer and Fiber Engineering (Dual minor in Chemistry and Materials), May 2013 - ***Georgia Institute of Technology***, [GPA-3.62/4.0]
- BSc. Chemical Engineering and Biotechnology, July 2008 – ***Mendeleyeev Univ. of Chem. Technology***, Moscow, Russia, [GPA- 5.0/5.0] (***Proficient in Russian Language***)
- Internet of Things- Roadmap to a connected world certification, May 2013- ***Massachusetts Institute of Technology*** Professional Education Digital Program

Professional Overview

Intel Corporation & Micron Corporation R&D (JDP) July 2016 to Date

Senior Integration Process TD Engineer, 2016-2017

Modeling/Simulation for electrical, FE-2-BE Tungsten interconnect, design layout as first-of-a-kind qualitative/quantitative predictive approach to electrical/die yield and EM/Reliability performance on 3D NAND technology nodes.

- Innovated a comprehensive statistical model for electrical layout and design for the 3D NAND technology that took into account upstream/down-stream processing variations for very accurate contact placement.
- The statistical Nature of the model was leveraged for predictive Electro-migration, Reliability and Electrical probe fails. (Over 3 weeks was gained by the R&D team due to the inline predictive model).

Intel Corporation, Hillsboro, OR July 2013 to 2016

Integration Process TD Engineer, 2015-2016

Back End and Far back end/Packaging process development for the Internet of Things (IOT) Technology. Packaging experience involved FCCSP-ETCSP/PTCSP, FCBGA, FCLGA and Technical interactions with laser scribing/dicing and Reliability R&D groups across intel campuses. Processing includes Cu Damascene FBE with/without Polyimide capping including Solder plating.

- Drove the development of the new Solder on Wafer/Bumping FBE/C4 process for the IOT technology with potential to reduce cost while maintaining reliability.
- Drove the development of a new ILD treatment that enabled the move to a CDO with higher thermo-mechanical stability for use in all lower layer BE for IOT.
- Drove the development and qualification of a new Etch-Stop material that enabled design rule relaxation for the lower-layer BE for the IOT technology node.
- Ran New product Introduction (NPI) Assembly test chip vehicle that is currently in-use for rel. testing for FBE/C4 for IOT
- Co-ordinating process flow/route creation for the BE/FBE for the IOT technology node

Integration Process TD Engineer, July 2013- September 2015

Back-End and Capacitor on Bit (COB) process development for the eDRAM technology node

- Successfully drove and implemented process changes to eliminate several yield limiting defect modes, including over-polish defect modes and corrosion defect modes, on the eDRAM (Capacitor on Bit) TD baseline.
- Successfully coordinated the implementation of new etch process at COB that resulted in complete COB defect elimination and allowed for over 50% more tool availability in the COB loop.
- Succesfully implemented custom edge processing on eDRAM for yield improvement by 0.2EISO
- Successfully coordinated and championed the smooth transfer of the eDRAM technology from R&D (Intel's TD factory in Hillsboro) to HVM mode (Intel's HVM factory in Arizona).
- Wrote/Published a comprehensive p1271.3 eDRAM yield transfer package and eDRAM integration transfer package to the VF -F32 in Arizona.
- Successfully worked with Intel, Arizona to close on defects post transfer of eDRAM to F32.
- Successfully drove and implemented process fix that increased the capacitance (~5%) at constant leakage on eDRAM thus allowing for FE Transistors to meet UPF targets.

Yield Analysis and Integration Process Engineer, December 2014 – April 2015

Yield Analysis for the eDRAM technology node

- Successfully used IdealPravda, Crystallball, YodaCreek, JMP for EOL raster level data analysis for eDRAM to enable better understanding of baseline systematic issues. This led to custom edge processing on eDRAM that increased yields by eliminating inline utilization dependent variations.

Georgia Institute of Technology, Atlanta, GA August 2009 – May 2013

Graduate Research Assistant, Direct Digital manufacturing Laboratory

- *Nanolithography*- Successfully used a novel, inexpensive advanced patterning with laser interference ablation to generate functional hierarchical metallic and ceramic nano masks with sub-40nm features on Si, SiO2, Si3N4 substrates
- *Stereo-Lithography*- Succesfully developed low-shrink photoactive material systems with epoxy, epoxy-acrylates, vinylethers, vinylether-acrylates, acrylates for use in 3D rapid

fabrication of composite airfoil molds designated for single-crystal casting of airfoil blades (DARPA funded project in collaboration with PCC Airfoils in Ohio)

DDM Systems, Atlanta, GA May 2013 - July 2013

Research and Development Intern

- Design and development of materials systems for rapid-prototyping of industrial scale airfoil moulds for high-temp. casting of Ni-super-alloys for turbine blades.

3M, Saint Paul, MN May 2012 – August 2012

Research and Development Technical Intern

- Synthesis/bio-analysis of fluorescing, carbohydrate-linked, organic molecules for the detection of E-Coli and Coliform micro-organisms. The novel material increased fluorescence intensity with optimal absorption coefficients at the emission maxima of conventional UV light sources.

Selected Publications, Awards and Recognitions

- Recognition for 3D NAND SC Capability enablement through predictive modelling and analysis with probe validation., **Q1 2017**
- LTD Divisional Award in recognition of outstanding contributions to developing a new CEE process for eDRAM improving yields by 2dpw, **Q3 2014**
- Best Student Paper Presentation Award at the TMS Conference, **April 2012**
- **Honorable Mention:** Gallery of 2013 **TMS** Micrograph Project Entries: http://www.tms.org/pubs/journals/JOM/micrographs.aspx
- F11FF NSF Travel Scholarship Award Recipient for MRS conference in Boston, **December 2011**
- Best poster presentation at the Georgia Tech Graduate Technical Symposium, **March 2012**
- First Class Honours degree - Mendeleyev Uni. of Chemical Technology, **July 2008**
- Bilateral Educational Award Scholarship recipient –Nigerian/Russian Governments, **2002**
- Best Science Student Award - Lagos State Model College Meiran, **2001**
- **Taiwo R. Alabi**, Dajun Yuan, David Bucknall and Suman Das; "Silicon Oxide Nanoforest: Novel Fabrication Technique and Applications" ACS Applied Materials and Interfaces. 2013, 5 (18), pp(8932-8938).
- **Taiwo R. Alabi**, Dajun Yuan, and Suman Das; "Hierarchical Metallic and Ceramic Nanostructures from Laser Interference Ablation and Block Copolymer Phase Separation" Nanoscale, 2013,5, 3912-3917.
- Krishna P. Acharya, **Taiwo R. Alabi**, Nicholas Schmall, Nishshanka N. Hewa-Kasakarage, Maria Kirsanova, Alexander Nemchinov, Elena Khon and Mikhail Zamkov, "Linker-free modification of TiO_2 nanorods with PbSe nanocrystals" Journal of Physical Chemistry C, (2009), 113 (45), 19531-19535.
- Krishna P. Acharya, Nishanka N. Kasakarage, **Taiwo R. Alabi**, Nemitz Ian, Elena Khon, Brunno Ullrich, Pavel Anzenbacher, Mikhail Zamkov, "Synthesis of PbS/TiO_2 colloidal Heterostructures for Photovoltaic Applications" Journal of Physical Chemistry C, (2010), 114 (29), 12496-12504.
- John W. Halloran, Vladislava Tomeckova, Susan Gentry, Suman Das, Paul Cilino, Rui Guo, Andirudh Rudraraju, Peng Shao, Tao Wu, **Taiwo R Alabi**, Daira Legdzina, Dennis Wolski, Walter R Zimbeck and David Long, "Photopolymerization of powder suspensions for shaping ceramics" Journal of the European Ceramic Society, (2011), 31(14), 2613-2619