GANESH SUNDARARAJAN

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SUMMARY

A highly accomplished DESIGN/VERIFICATION ENGINEER with extensive experience in front-end RTL design in various technologies such as wireless MODEM (CDMA, WCDMA), imaging, data network, memory interfaces (WideIO), pre- and post-silicon verification strategy formulation and execution, embedded processor design aspects, and ASIC/FPGA design methodologies (front and backend flow). Possess a proven track record in converting concepts to products both as an individual contributor as well as a team leader. Worked with cross-functional teams including systems/architecture/SW teams to define specifications and successful completion of projects

TECHNICAL SKILLS

- **Languages:** System Verilog**,** Verilog, VHDL, System-C, C, C++, Perl, TCL, QuickCov (functional coverage), PSL/Sugar (Assertion Based Verification), PythonSV, Matlab
- **Simulation Tool:** NCSIM, Modelsim, NCVerilog
- **Silicon Validation Environment:** Ti Top-Sim Env
- **Synthesis:** Cadence, Synopsys, Synplify
- **RTL linting**: Spyglass
- **Static Timing Analysis:** Primetime
- **ASIC Vendor:** Agere Systems, Texas Instruments, AMI
- **Emulation Platform:** Veloce (Mentor)
- **FPGA:** Xilinx, Altera, Actel, Lattice

PATENTS & HONORS

- WIPO Patent WO2012068449: CONTROL NODE FOR A PROCESSING CLUSTER, May 2012, Texas Instruments Inc.
- WIPO Patent WO2012068486: LOAD/STORE CIRCUITRY FOR A PROCESSING CLUSTER, May 2012, Texas Instruments Inc.
- WIPO Patent WO2012068475, WO2012068498: METHOD AND APPARATUS FOR MOVING DATA FROM A SIMD REGISTER FILE TO GENERAL PURPOSE REGISTER FILE, May 2012, Texas Instruments Inc.
- WIPO Patent WO2012068478: SHARED FUNCTION-MEMORY CIRCUITRY FOR A PROCESSING CLUSTER, May 2012, Texas Instruments Inc.
- WIPO Patent WO2012068494: CONTEXT SWITCH METHOD AND APPARATUS, May 2012, Texas Instruments Inc.
- United States Patent, 13/232,774, "High-Performance, Scalable Multicore Hardware and Software System". Filing date September 14, 2011, William Johnson, Murali Chinnakonda, Jeffrey Nye, Toshio Nagata, John Glotzbach, Hamid Sheikh, Ajay Jayaraj, Stephen Busch, Shalini Gupta, Robert Nychka, David Bartley, Ganesh Sundararajan; Texas Instruments Inc.
- United States Patent 8155089 for "System and Method of Processing CDMA Signals". April 10, 2012, Inventor: Ganesh Sundararajan, Xixian Chen, Woon Thong, Edward Mah and Karl Mann; Ericsson AB.
- United States Patent "CDMA Probe for Self-Testing Base Station Receivers", Filed June 26, 2004 (http://www.wipo.org/pctdb/en/wo.jsp?wo=2006007714). Inventor: Ganesh Sundararajan, Edward Mah, Neil McGowan; on behalf of NORTEL Networks.
- United States Patent 7173900 "Method and Apparatus For Chip Generation of a Chip Sequence". Feb 2, 2007 (http://www.patentstorm.us/patents/7173900.html). Inventor: Ganesh Sundararajan; on behalf of NORTEL Networks.
- United States Patent filed for "System and Method of Processing CDMA Signals". June 3, 2003, Inventor: Xixian Chen, Woon Thong, Ganesh Sundararajan, Edward Mah and Karl Mann; on behalf of NORTEL Networks.
- Awarded Technical Excellence Certificate for year 2001 at NORTEL.
- First Class with Distinction in B. Eng (Fourth Rank).

EXPERIENCE

INTEL Corporation, USA

Santa Clara USA, 2013-2014
Senior Electrical Engineer ……Present

Responsible for Intel wearable's Platform validation under the charter of IoT.

Austin, Texas
Senior Validation Engineer 2013-2014

- **Senior FPGA Design Engineer for ATOM Validation:** Worked on Injector FPGA designs that validate ATOM peripherals like DDR, I2S, etc
- **Senior Emulation Validation Engineer:** Working on emulation validation of Intel ATOM Softcore bridges (OCP, AXI), Core-DFX Debug script developer

TEXAS INSTRUMENTS INC, Dallas, Texas, USA
Senior ASIC Design Engineer..... 2006-2013

- **Design Lead for WideIO Memory Interface Controller, 2011-2012:** Performed work involving interfacing with systems/architecture team on definition of WideIO interface architecture, RTL development, verification (multisited), synthesis for timing closure, of IP (as part of Integrated Memory System).
- **Module Developer for Imaging Sub-System of OMAP6, 2011-2012:** Involved in RTL development/re-architecting/update of various ISS (Imaging Sub-System) IP modules (OCP2OCP pipes, Bayer Scaler, H3A statistics Module). Worked with multisited verification teams for design closure.
- **Design Engineer, Torrent Programmable Image Cluster, 2009-2011:** Involved in definition/design/verification (multisited) of IP blocks (Global Load Store, Control Node) for Torrent Programmable Image Cluster (TPIC) sub-system. Worked with architect for integrating simple instruction Torrent RISC processor into the Global Load Store IP.
- **OMAP4430–Silicon Validation Engineer for Imaging Sub-system, 2008-2009:** Involved in development of new methodology for validating OMAP4430 imaging sub-system for pre- and post-Si-verification. Developed XLS-based test case definition/development/verification strategy to perform end-to-end testing of imaging pipe. Test methodology helped identify pre-silicon bugs on emulation platform/ Testcases also helped quick Silicon bringup of imaging subsystem before SW team engagement.
- **Wrigley 3G chip-set Development, Lead Engineer, 2006-2008:** Performed work involving taking on different tasks as design lead for module and symbol chain design/verification, FPGA team support, and SW/lab support. Performed RTL development including modifications to Turbo/Viterbi decoders, HARQ, MBMS hardware architecture development, Release-7 CPC architecture development, and transmitter. Worked with end-customer for product launch and knowledge transfer.

NORTEL NETWORKS, Ottawa, Canada
FPGA/ASIC Lead Design Engineer 1996-2006

- **CDMA Wireless Development, Design Prime, 2004-2006:** Served as technical lead of four-person FPGA project; developed interface FPGA as part of 1xEV-DO (Data Only) channel element module development.
- **Module Designer, Wireless Technology Leadership, 2003-2005:** Served as part of ASIC team, with responsibilities including developing IS-95 Access-Probe module simulating mobile access-probe channel for NORTEL CDMA base-station test. Performed work involving RTL development, verification, FPGA prototyping, system test and post-ASIC verification.
- **CDMA Wireless Development, Design Prime, 2004-2005:** Served as technical lead of three-person team; addressed product obsolescence of HDLC ASIC on Selector Bank Sub-System Controller. Worked on project involving designing drop-in replacement for original ASIC via FPGA, and then converting into ASIC. Developed adaptor card with same footprint of original ASIC housing FPGA for RTL development, adaptor card design leadership, lab-debug and ASIC conversion.
- **Wireless Technology Leadership, 2002-2003:** Served as part of second generation GPS Timing Module development team; involved in developing configuration CPLD and GPS Timing FPGAs.
- **CDMA Development, 2002-2003:** Involved in development of next generation enhanced CEM (Channel Element Module). Performed RTL development of FPGA-titled (BIR), generating design document, simulation plan/report, design verification, RTL and gate-level simulation, and lab verification. Designed Segmentation and Reassembly (SAR) FPGA for NORTEL Basestation Communication Network (BCN) to handle control information protocol.
- **Project Lead**, **IXEV-DV/CDMA-2000 MODEM Development, 2000-2003:** Led technology demonstrator project involving design and development of NCM (NORTEL Cell-site MODEM) ASIC/FPGA for 1xRTT/1xEV-DV. Performed work involving definition of MODEM architecture (design of transmitter), RTL development, synthesis and other back-end work. Served as Project lead for receiver and as designer of IS-2000 transmitter.

- **Architect, CDMA Development-Cost Reduction, 2002:** Defined architecture of emulator card for testing Channel Element cards to replace base-stations at manufacturing sites. Involved in writing test-proposal, development of general specification, detailed design document.
- **Design Prime, CDMA Development, 1999-2000:** Involved in design of MODEM interface FPGA/ASIC for CDMA Channel Element Module (CEM). Created initial product FPGA-based CEM using Xilinx Virtex XCV300, with FPGA interfacing QUALCOMM CSM-5000 MODEM (CDMA 2000, IS-95) ASIC with Nortel's wireless base-station. Involved in design of FPGA, definition of CEM card, and definition of SW interface, lab verification and field support. Involved in converting FPGA developed in 2000 to ASIC (approximately 75K gate-count); performed back-end work in ASIC flow such as static timing closure, gate-level simulation, and functional test-vector generation for ASIC tester.
- **ASIC Design Engineer, OC-48 Development, 1996-1999:** Involved in design of ASICs for OC-48 (SONET) product. Performed work involving design of various new blocks in chip, simulation, timing analysis (multi-clock domain analysis), test pattern generation for chip fabrication, lab verification of features, and firmware/software support.

A D D I T I O N A L E X P E R I E N C E

ZEITNET, (a Cabletron Systems Company), Santa Clara, California, USA, **Member Technical Staff (ASIC/FPGA)**,1994-1996. Performed work involving design of ATM adapter cards and ATM Switching fabric.

SOLFLOWER COMPUTER INC., San Jose, California, USA, **Design Engineer**, 1992-1994. Performed work involving design of SBus-VME adapter card, SCSI storage system.

OKLAHOMA STATE UNIVERSITY, Stillwater, Oklahoma, **Research Assistant**, **Department of Electrical Engineering,** 1990-1991.

E D U C A T I O N

UNIVERSITY OF PHOENIX, Phoenix, Arizona, **M.B.A., Technology Management,** 2005

OKLAHOMA STATE UNIVERSITY, Stillwater, Oklahoma, **M.S., Electrical and Computer Engineering,** 1992

ANNAMALAI UNIVERSITY, Chidambaram, Tamil Nadu, India, **B.E. Electronics and Instrumentation,** 1988

A F F I L I A T I O N S

Member of Tau Beta Phi, Engineering Honor Society, Oklahoma State University

Member of Eta Kappa Nu, Electrical Engineering Honor Society, Oklahoma State University